CLAIMS

What is claimed is:

1. An apparatus comprising:

a planarized metal interconnect line as the ultimate interconnect layer of an integrated circuit, the planarized metal interconnect line coupled to a bottom electrode of an electrically decoupling capacitor wherein a top electrode of the electrically decoupling capacitor is coupled to a flip chip bump contact such that the capacitor is disposed between and aligned between at least a portion of the metal interconnect line and the bump contact.

2. The apparatus of Claim 1, wherein the bump contact contacts the top electrode of the decoupling capacitor through multiple bumps.

3. The apparatus of Claim 1, wherein the bottom electrode and the top electrode comprise a material that acts as an oxidation and diffusion barrier.

4. The apparatus of Claim 1, wherein a dielectric material having a dielectric constant greater than silicon dioxide comprising the top electrode and the bottom electrode are separated by one of tantalum pentoxide (Ta_2O_5), Barium Strontium Titanate (BST) and Silicon Nitride (SiN).

5. The apparatus of Claim 4, wherein when the dielectric material is Barium Strontium Titanate the bottom electrode and the top electrode material comprises one of Platinum (Pt), Ruthenium (Ru) and Iridium (Ir).

6. The apparatus of Claim 1, wherein the bottom electrode and the top electrode material comprises one of Tantalum Nitrate (TaN), Titanium Nitrate (TiN), Tungsten Nitrate (WN).

7. An apparatus comprising:

an integrated circuit having a top metal layer interconnect as the ultimate interconnect layer of an integrated circuit, the top metal layer having a plurality of voltage bias lines with a plurality of voltage bias purposes;

a decoupling capacitor coupled to a first top metal voltage bias line;

a bump contact coupled to the decoupling capacitor and a second top metal voltage bias line such that the capacitor is disposed between and aligned between at least a portion of the first top metal voltage bias line and the bump contact, the second top metal voltage bias line having a different purpose than the first top metal voltage bias line coupled to the capacitor, wherein the bump contact provides power to the second metal voltage bias line and electrically decouples the first metal voltage bias line from the second metal voltage bias line.

8. The apparatus of Claim 7, wherein the decoupling capacitor comprises:

a bottom electrode coupled to a top metal voltage bias line;

a dielectric material having a dielectric constant greater than that of silicon dioxide coupled to the bottom electrode; and

a top electrode coupled to the dielectric material.

9. The apparatus of Claim 8, wherein the bottom electrode and the top electrode comprise a material that acts as an oxidation and diffusion barrier.

10. The apparatus of Claim 8, wherein the dielectric material used in the decoupling capacitor comprises one of tantalum pentoxide (Ta_2O_5), Barium Strontium Titanate (BST) and Silicon Nitride (SiN).

11. The apparatus of Claim 10 wherein when the dielectric material is Barium Strontium Titanate the bottom electrode and the top electrode material comprises one of Platinum (Pt), Ruthenium (Ru) and Iridium (Ir).

12. The apparatus of Claim 7, wherein the bottom electrode and the top electrode material comprises one of Tantalum Nitrate (TaN), Titanium Nitrate (TiN), Tungsten Nitrate (WN).

13. An apparatus comprising:

an integrated circuit having a layer of metal interconnect as the ultimate interconnect layer of the integrated circuit;

a decoupling capacitor stack on the layer of metal interconnect; and

a bump contact contacting the capacitor stack such that the capacitor stack is disposed between and aligned between at least a portion of the layer of metal and the bump contact.

14. The apparatus of Claim 13, wherein the capacitor stack comprises:

a high coefficient of permittivity material, and a top electrode.

15. The apparatus of Claim 14, wherein the capacitor stack further comprises a bottom electrode.

16. The apparatus of Claim 15, wherein the bottom electrode and the top electrode comprise a material that acts as a diffusion barrier to the metal layer.

17. The apparatus of Claim 16, wherein the bottom electrode and the top electrode comprise a material that acts as a diffusion barrier to oxygen.

18. A apparatus comprising:

an integrated circuit comprising a layer of metal as the ultimate interconnect layer of the integrated circuit,

a capacitor stack comprising:

a blanket bottom electrode material on the layer of metal,

a dielectric material having a dielectric constant greater than that of silicon dioxide on the blanket bottom electrode material,

a blanket top electrode material on the dielectric material,

a blanket passivation layer on the stack, and

a bump contact contacting the top electrode material such that the top electrode material is disposed between and aligned between at least a portion of the layer of metal and the bump contact.

19. The apparatus of Claim 18, wherein the bottom electrode and the top electrode comprise a material that acts as an oxidation barrier.

20. The apparatus of Claim 18, wherein the bottom electrode and the top electrode comprise a material that acts as a diffusion barrier.

21. The apparatus of claim 18, wherein the bump contact is in direct physical contact with the top electrode.

22. An apparatus comprising:

an integrated circuit having a layer of metal interconnect as the ultimate interconnect layer of the integrated circuit, wherein the layer of metal comprises a first metal power bias voltage line and a second metal power bias voltage line;

a decoupling capacitor stack on a portion of the first metal power bias voltage line, the decoupling capacitor having a characteristic to reduce a voltage droop on the first metal power bias voltage line;

a passivation layer over a top and a side of the decoupling capacitor stack;

a bump contact contacting the capacitor stack through a removed portion of the passivation layer over the top of the decoupling capacitor stack such that the capacitor stack is disposed between and aligned between at least a portion of the layer of metal and the bump contact, the bump contact also contacting the second metal power bias voltage line.

23. The apparatus of Claim 22, wherein the capacitor stack comprises:

a high coefficient of permittivity material, and a top electrode.

24. The apparatus of Claim 23, wherein the capacitor stack further comprises a bottom electrode.

25. The apparatus of Claim 24, wherein the bottom electrode and the top electrode comprise a material that acts as a diffusion barrier to the metal layer.

26. The apparatus of Claim 25, wherein the bottom electrode and the top electrode comprise a material that acts as a diffusion barrier to oxygen.